the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

electrically coupling said first active surface to said substrate with at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pad; and

securing said first stacking surface to said second stacking surface.

21. (Cancelled)

22. (Cancelled)

23. A method of assembling a printed circuit board, said method comprising:

providing a substrate including first and second surfaces and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads;

securing said first stacking surface to said first surface of said substrate between said conductive contacts included on said first surface of said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes a plurality of conductive bond pads;

electrically coupling said first semiconductor die to said second semiconductor die with a plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface;

securing a single decoupling capacitor to said second stacking surface;

providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said first active surface, and a conductive contact on said first surface of said substrate;

electrically coupling said bond pad on said first active surface to said second semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface;

arranging said pair of conductive lines such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and

providing a plurality of topographic contacts extending from said second surface of said substrate to said first surface of said printed circuit board.

24. A method of assembling a printed circuit board, said method comprising:

providing a substrate including a first surface and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes a plurality of conductive bond pads;

electrically coupling said first active surface to said substrate with a plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads;

securing said first stacking surface to said second stacking surface;

securing a single decoupling capacitor to said second stacking surface;

providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate;

electrically coupling said conductive contact on said first surface of said substrate to said first semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate;

arranging said pair of conductive lines such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and

providing a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

45-51. (Cancelled)

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52. (New) A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate including a first surface and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

securing said first stacking surface to said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pad;

electrically coupling said first semiconductor die to said second semiconductor die with at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface;

securing at least one decoupling capacitor to said second stacking surface; and

providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said first active surface, and a conductive contact on said first surface of said substrate.

53. (New) The method as claimed in claim 20 further comprises providing at least one conductive line extending from a bond pad on said second active surface to a conductive contact on said first surface of said substrate.

54. (New) A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate including a first surface and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

electrically coupling said first active surface to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said first surface of said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pad;

securing said first stacking surface to said second stacking surface;

securing at least one decoupling capacitor to said second stacking surface; and

providing at least one conductive line connecting said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate.

55. (New) A method of assembling a printed circuit board, said method comprising:

providing a substrate;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

electrically coupling said first active surface to said substrate by at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said substrate;

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providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pads;

securing said first stacking surface to said second stacking surface;

positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and

providing a plurality of topographic contacts extending from said second surface of said substrate to said first surface of said printed circuit board.

56. (New) The method as claimed in claim 54 further comprising providing at least one conductive line extending from a bond pad on said second active surface to a conductive contact on said first surface of said substrate

REMARKS

By the present amendment, claims 19, 21, 22 and 45-51 have been cancelled. Original claims 20, 23 and 24 are pending in the present application. New claims 52-56 have been added.

CONCLUSION

Applicant respectfully submits that the application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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